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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/186,973	11/05/1998	KATHERINE G. HEINEN	1000-2035	2495

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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/186,973	HEINEN ET AL.	
	Examiner	Art Unit	
	Suk-San Foong	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 14-15, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arima et al. ('151) in view of Khandros et al. ('861) and Dalal et al. ('423) and further in view of DiStefano et al. ('764) as previously applied, and further in view of Dalal et al. ('268).

The teachings of Arima et al., Khandros et al., Dalal et al. ('423) and DiStefano et al. are relied on for the teachings discussed in the rejections of paragraph 3 of the Office Action mailed on 8/14/02.

The combination process does not disclose applying radiant energy to a second surface of semiconductor wafer.

Dalal et al. ('268) discloses a method of attaching integrated circuit chip to an interposer which includes proving interposer 25 (Col. 4, lines 10-14, Col. 7, lines 2-9), then providing IC chip 30 with solder balls 38 (Col. 8, lines 4-6, and Fig. 4), subsequently joining interposer 25 with IC chip 30 through solder balls 38 of IC chip 30 (Col. 8, lines 6-13), and subsequently reflowing solder balls 38 by applying radiant energy to IC chip 30, hence, to a second surface of IC chip 30 (Col. 9, lines 14-17).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Dalal et al. ('268) with the combination process because it would enable formation of the physical bonds between the solder ball 10 and ports 11 and 12 to be performed.

The choice of range in temperature to cause solder balls to reach a liquid state would have been a matter of routine optimization to achieve the desired device and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being obvious over Arima et al. ('151) in view of Khandros et al. ('861) and Dalal et al. ('423) and further in view of DiStefano et al. ('764) as previously applied, and further in view of Amador et al. ('744).

The combination process does not disclose that an adhesive layer having a multitude of electrically conductive fibers wherein fibers are arranged in the adhesive layer at a second spacing pitch and the second pitch being smaller than the first pitch.

Amador et al. discloses an adhesive film containing conductive fibers to connect chip 13 with interposer 16 wherein the fibers are arranged in the adhesive layer at a second spacing pitch

and the second pitch being smaller than the first pitch (Col. 10, line 48 to Col. 11, line 30, and Fig. 12).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Amador et al. with the combination process because it would enable formation of conductive paste in place of solder balls 12 of Arima et al. in the process of the combination to be performed.

Response to Arguments

5. Applicant argues that DiStefano does not disclose a semiconductor device. However, applicant is directed to Col. 1, lines 34-38 of DiStefano et al wherein integrated circuits such as semiconductor chips can be mounted to circuit panels.

6. Applicant argues that Arima et al. fails to disclose semiconductor wafers. However, Arima et al. is not relied on for this teaching. Dalal et al. ('423) is relied on for this teaching as stated in paragraph 2 of the Office Action mailed on 3/14/02.

7. Applicant argues that Khandros et al. teaches forming solder balls on the interposer as opposed to chip. However, applicant is directed to Col. 12, lines 15-26 wherein solder balls are formed on chip.

8. Applicant argues that Dalal et al. ('423) teaches mounting a chip to an interposer with a lone references stating that the chip could be a wafer. The additional teachings of Dalal et al. ('423) does not negate those relied on.

Allowable Subject Matter

9. If claims were submitted limited to heating the wafer and the interposer by simultaneously applying separately controlled, different intensity or wavelength radiant energy to the side of the wafer on which the interposer is placed as opposed to the opposite side of the wafer to minimize differences in thermal expansion would be allowed.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

March 9, 2003

George Fourson
Primary Examiner
Art Unit 2823